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Kuestion

Analog and Digital Electronics

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Contents

Manual for Kuestion

Why Kuestion?

It's very overwhelming for a student to even think about finishing 100-200 questions per chapter when the clock is ticking at the last moment. This is the reason why Kuestion serves the purpose of being the bare minimum set of questions to be solved from each chapter during revision.

What is Kuestion?

A set of 40 questions or less for each chapter covering almost every type which has been previously asked in GATE. Along with the Solved examples to refer from, a student can try similar unsolved questions to improve his/her problem solving skills.

When do I start using Kuestion?

It is recommended to use Kuestion as soon as you feel confident in any particular chapter. Although it will really help a student if he/she will start making use of Kuestion in the last 2 months before GATE Exam (November end onwards).

How do I use Kuestion?

Kuestion should be used as a tool to improve your speed and accuracy chapter wise. It should be treated as a supplement to our K-Notes and should be attempted once you are comfortable with the understanding and basic problem solving ability of the chapter. You should refer K-Notes Theory before solving any "Type" problems from Kuestion.

Type: 1 Diode Circuits

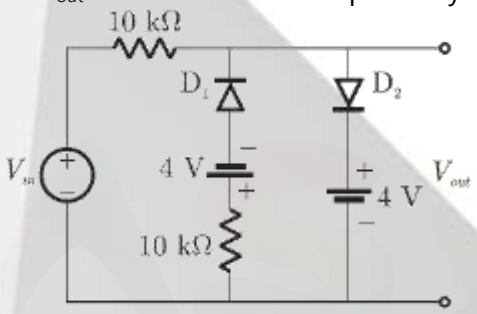
For Concepts, please refer to Analog Electronics K-Notes, Diodes

Point to Remember:

Remember to check the state of other diode after assuming state of one diode to verify the initial hypothesis.

Sample Problem: 1

A voltage signal 10 sinωt is applied to the circuit with ideal diodes, as shown in figure, the maximum, and minimum values of the output waveform V_{out} of the circuit are respectively



(A) +10 V and −10 V

(B) +4 V and −4 V

(C) +7 V and −4 V

(D) +4 V and −7 V

Solution: (D) is correct option

In the positive half cycle (when Vin > 4 V) diode D_2 conducts and D_1 will be off so the equivalent circuit is, Vout = + 4 Volt

In the negative half cycle diode D_1 conducts and D_2 will be off so the circuit is,

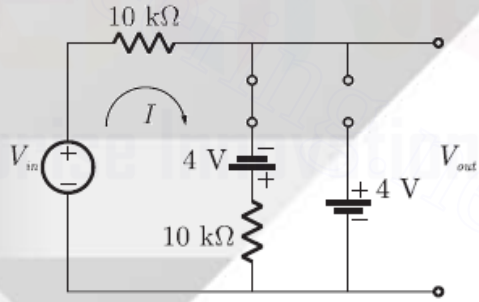
Applying KVL

$V_{in} - 10I + 4 - 10I = 0$

$\frac{V_{in}+4}{20} = I$

$V_{in} = -10$ V (Maximum value in negative half cycle)

So, $I = \frac{-10+4}{20} = -\frac{3}{10}$ mA

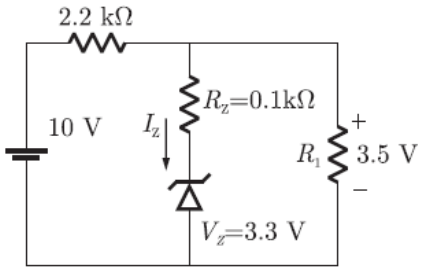


$\frac{V_{in}-V_{out}}{10} = I$

$\frac{-10-V_{out}}{10} = -\frac{3}{10} \Rightarrow -(10-3) \Rightarrow -7$ volt

Sample Problem: 2

The current through the Zener diode in figure is



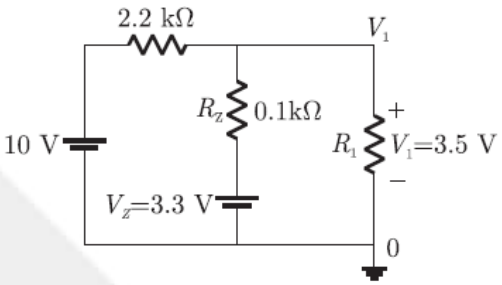
(A) 33 mA (B) 3.3 mA

(C) 2 mA (D) 0 mA

Solution: (C) is correct option

Given circuit
In the circuit
V_1 = 3.5 V (given)
Current in zener is.

$$I_z = \frac{V_1 - V_z}{R_z} = \frac{3.5 - 3.3}{0.1 \times 10^3} = 2 \text{ mA}$$



Unsolved problems:

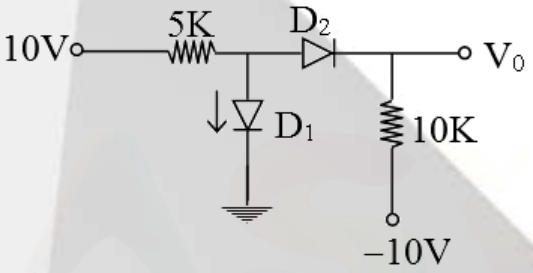
Q.1 Assume that each diode has V_γ = 0.7V for the circuit shown below. The current passing through the diode D_1 is

(A) 0

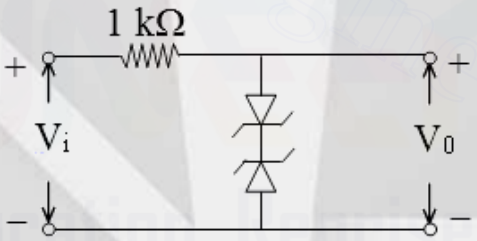
(B) 0.86 mA

(C) 1 mA

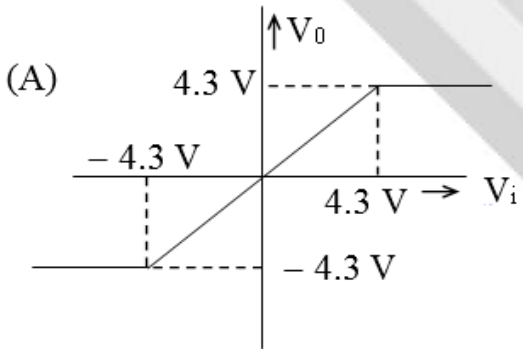
(D) 1.86 mA



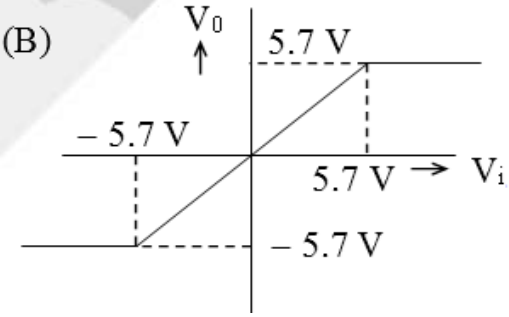
Q.2 For the circuit shown below, the Zener diode has $V_Z = 5V$ and the $V_\gamma = 0.7V$ when it is forward biased. The transfer characteristic curve is



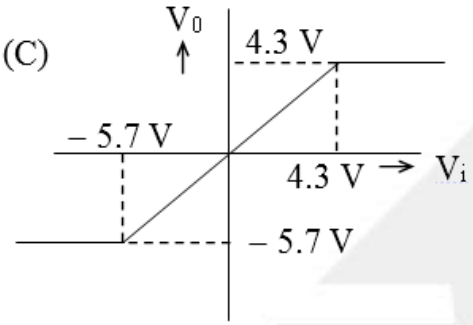
(A)



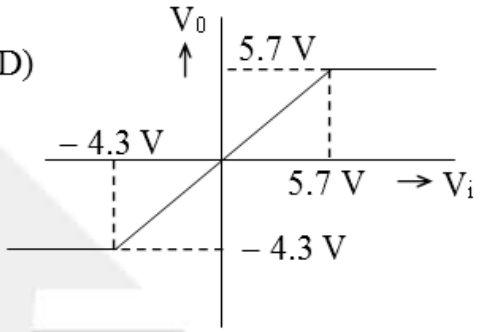
(B)



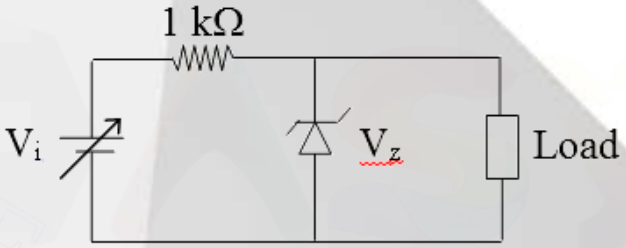
(C)



(D)



Q.3 The Zener diode in the circuit shown has V_z = 6.2 V and Zener knee current is 5 mA. The maximum load current drawn from this circuit ensuring proper functioning over input range (40 – 50V) is



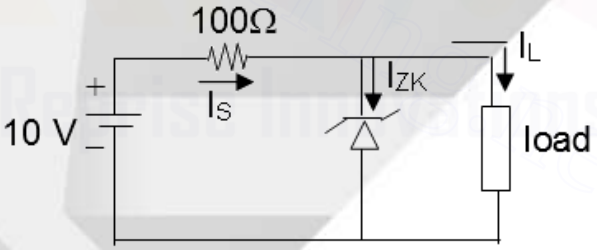
(A) 43.8 mA

(B) 38.8 mA

(C) 33.8 mA

(D) 28.8 mA

Q.4 In the zener voltage regulator ckt shown in fig. the 5V zener diode requires I_{ZK} of 10mA for obtaining a regulated out-put fof 5V. The maximum permissible load current in the ckt and minimum power rating of zener diode respectively are



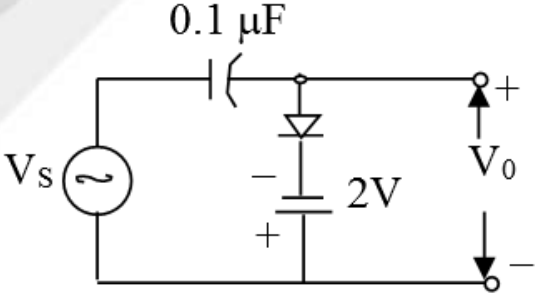
(A) 10mA, 0.25 watts

(B) 50mA, 0.25 watts

(C) 40mA,0.25 watts

(D) 40mA, 2.5 watts

Q.5 For an input of V_S = 5 sinωt, (assuming ideal diode), the ckt shown in fig. will behave as?



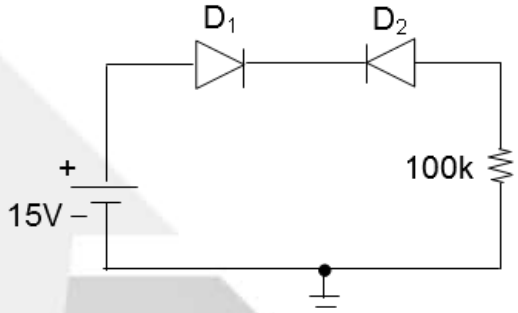
(A) Clipper, sine wave clipped at – 2V

(B) Clamper, sine wave clamped at – 2V

(C) Clamper, sine wave clamped at 0 volt

(D) Clipper, sine wave clipped at 2V

Q.6 Two identical junction diodes where V_I characteristics is I_s = 0.1 μA; V_T = 26 mV andη = 2 are connected as shown in fig. The voltage across diode 2 (D_2) will be



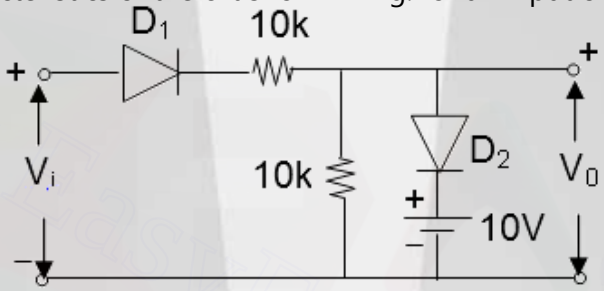
(A) 0.0347V

(B) 0.01 V

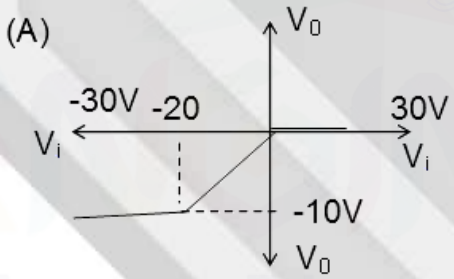
(C) 14.953 Volts

(D) 15 V

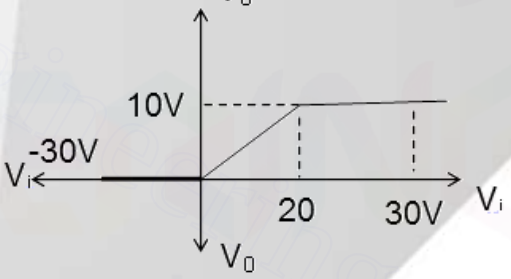
Q.7 The transfer characteristics of the ckt shown in fig. for an input of 30 sin ωt is



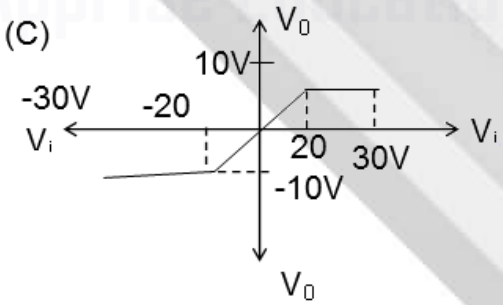
(A)



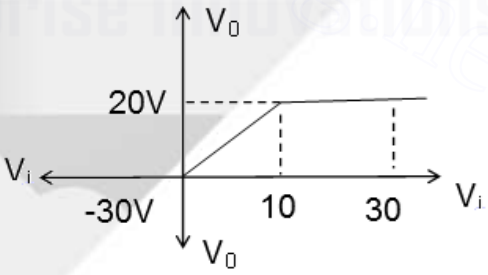
(B)



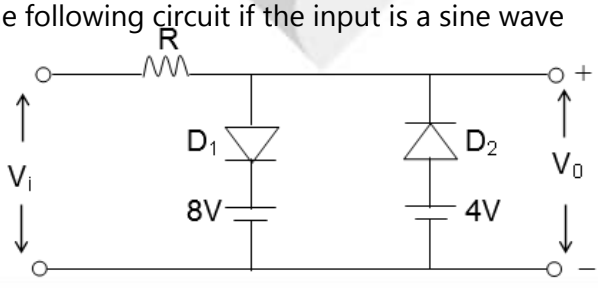
(C)



(D)



Q.8 The function of the following circuit if the input is a sine wave



(A)Transmits that part of sine wave, which is above + 8V and below + 4V.
(B)Transmits that part of sine wave, which lies between + 4V and + 8V.
(C)Transmits that part of sine wave, which lies above – 4V and below + 8V
(D)Transmits that part of sine wave, which lies below + 4V and above – 8V

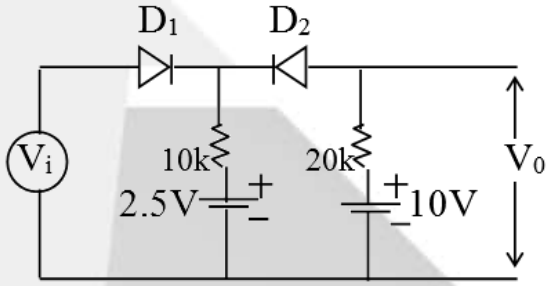
Q.9 For the clipper circuit shown in the Fig. the first break point occurs when V_i is at

(A) 2.5 V

(B) 5 V

(C) 10 V

(D) 7.5 V



Type: 2 BJT and FET Biasing

For Concept, refer to Analog Electronics K-Notes, Transistor Biasing and Transistor Amplifiers

Point to Remember:

Verify the region of operation of Transistor before calculating the Transistor parameters.

Sample Problem 3:

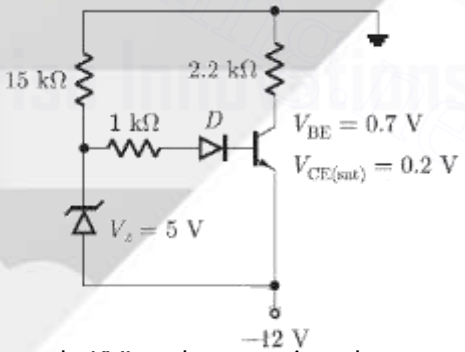
The transistor used in the circuit shown below has a β of 30 and I_{CBO} is negligible. If the forward voltage drop of diode is 0.7 V, then the current through collector will be

(A) 168 mA

(B) 108 mA

(C) 20.54 mA

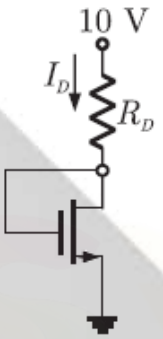
(D) 5.36 mA



Solution: (D) is correct option
Assume that the transistor operated in active region then apply KVL to base-emitter loop.
$5\text{-}10^3 I_B\text{-}0.7\text{-}0.7+12=0$
$I_B=15.6$ mA
$I_C=0.468$ A
Apply KVL to collector-emitter loop
$0\text{-}2.2K\ I_C\text{-}V_{CE}+12=0$
$V_{CE}=2200\ I_C\text{-}12=1017.6$ V

As $0<V_{CE}<V_{CC}$ Not satisfying this condition. Transistor operating in saturation region.
$V_+(sat)=0.2$ V
Apply KVL, $0-2.2I_C-0.2+12=0$
$I_C=5.36$ mA

Sample Problem 4:
For the n-channel enhancement MOSFET shown in figure, the threshold voltage V_{th} = 2 V. The drain current I_D of the MOSFET is 4 mA when the drain resistance R_D is 1 kΩ. If the value of R_D is increased to 4 kΩ, drain current I_D will become



(A) 2.8 mA

(B) 2.0 mA

(C) 1.4 mA

(D) 1.0 mA

Solution: (A) is correct option

For a n-channel enhancement mode MOSFET transition point is given by,
$V_{DS(sat)} = V_{GS} - V_{TH}$ (V_{TH} = 2 volt)
$V_{DS(sat)} = V_{GS} - 2$
From the circuit,
$V_{DS} = V_{GS}$
So $V_{DS(sat)} = V_{DS} - 2$ & $V_{DS} = V_{DS(sat)} + 2$
$V_{DS} > V_{DS(sat)}$
Therefore transistor is in saturation region and current equation is given by.
$I_D = K(V_{GS} - V_{TH})^2$
$4 = K(V_{GS} - 2)^2$
V_{GS} is given by
$V_{GS} = V_{DS} = 10 - I_D R_D$
$= 10 - 4 * 1 = 6$ Volt
So, $4 = K(6 - 2)^2$
$K=1/4$
Now R_D is increased to 4 kΩ, Let current is I'_D and voltages are $V'_{DS} = V'_{GS}$
Applying current equation.

$$I'_D = K(V'_{GS} - V_{TH})^2$$

$$I'_D = \frac{1}{4}(V'_{GS} - 2)^2$$

$$V'_{DS} = V'_{GS} = 10 - I'_D \times R'_D = 10 - 4I'_D$$

$4I'_D = (10 - 4I'_D - 2)^2 \Rightarrow 4I'_D = (8 - 4I'_D)^2$

So, $4I'_D = 16(2 - I'_D)^2$

$4I'^2_D - 17 + 16 = 0 \Rightarrow I'_D = 2.84$ mA

Unsolved Problems:

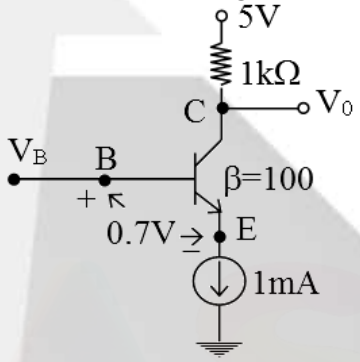
Q.1 For the transistor circuit shown below, the value of the output voltage V_o is

(A) 0.2 V

(B) 2.5 V

(C) 4 V

(D) 5 V



Q.2 Match the following:

List – 1	List – 2
P. JFET	1. Amplifier
Q. BJT	2. Operated in depletion mode only
R. D-MOSFET	3. Operated in enhancement mode only
S. E-MOSFET	4. Operated in both depletion and enhancement modes

Codes:

(A) P-2, Q-1, R-3, S-4
(B) P-3, Q-1, R-2, S-4
(C) P-4, Q-1, R-3, S-2
(D) P-2, Q-1, R-4, S-3

Q.3 The drain of an n-channel MOSFET is directly connected to Gate so that $V_{GS} = V_{DS}$. The threshold voltage of it is 2 V. The drain Current is 2mA, when $V_{GS} = 3V$. Then for $V_{DS} = 4V$, the value of I_D is

(A) 8 mA
(B) 4 mA
(C) 2.67 mA
(D) 1.5 mA

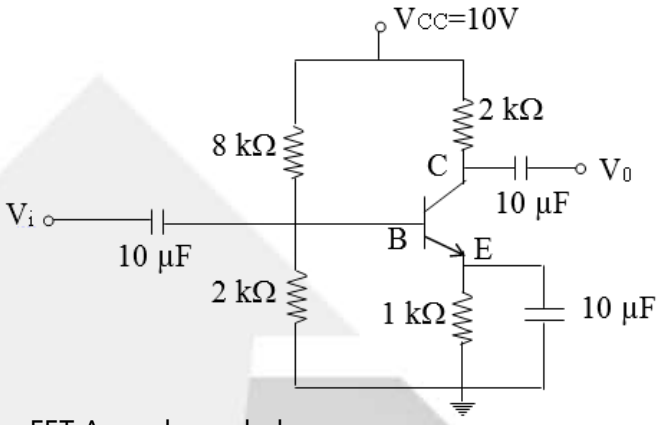
Q.4 For the transistor circuit shown below $h_{fe} = \beta = 100$, $h_{ie} = 1$ kΩ. The DC voltage between the collector and emitter terminals is

(A) 2.52 Volts

(B) 5 Volts

(C) 6.207 Volts

(D) 7.48 Volts



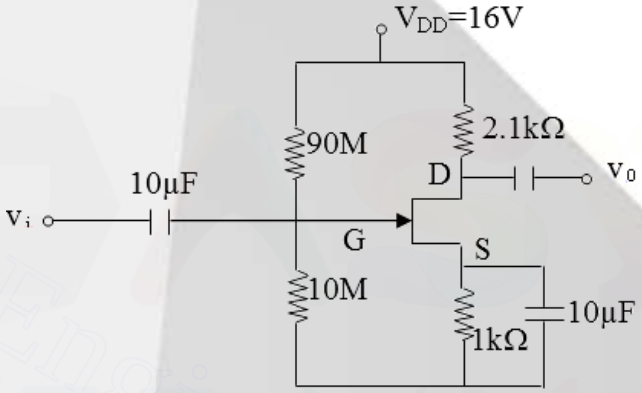
Q.5 Calculate the voltage gain A_v for the FET Amp shown below.
Assume I_{DSS} = 8mA, r_d=90kΩ, V_P=-6V.

(A) -3.65

(B) -9.11

(C) -1.07

(D) -10.74



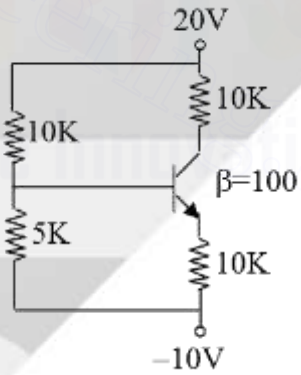
Q.6 In the transistor circuit given that β = 100, V_{BE} = 0.7 The value of Quiescent collector current & voltage are

(A) (0.589 mA, 18.22 V)

(B) (0.917 mA, 11.56 V)

(C) (11.56 V, 0.589 mA)

(D) (18.22 V, 0.917 mA)



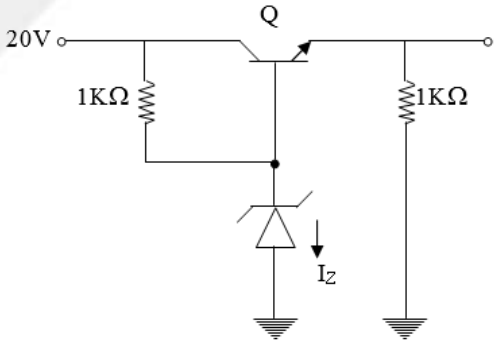
Q.7 In the Series voltage regulator circuit. Given that V_Z = 10 V, V_{BE} = 0.7 V, β=50.
The value of V_{CE} = ...

(A) 20 V

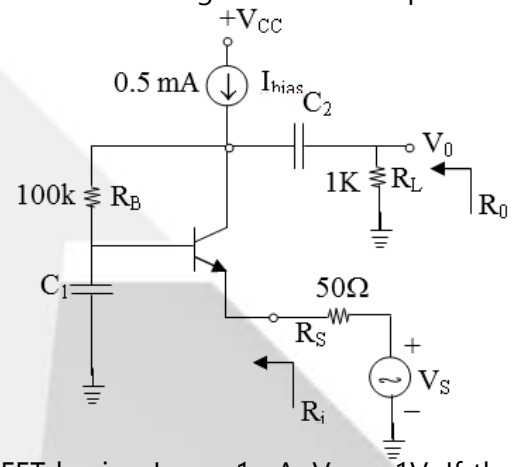
(B) 10 V

(C) 9.3 V

(D) 10.7 V



Q.8 A BJT amplifier is shown in fig. Assume that the current I_{bias} is ideal, and the transistor has very largeβ, $r_b = 0$ and $r_0 \to \infty$. The small signal ac mid band gain of the amplifier is (approximately)



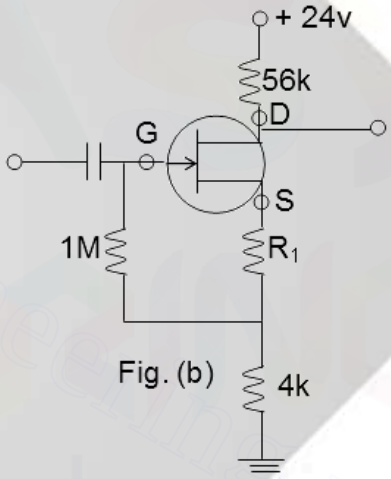
(A) 100

(B) 50

(C) 20

(D) 1

Q.9 The amplifier stage shown uses an n – channel FET having $I_{DSS} = 1mA$, $V_P = -1V$. If the quiescent to ground voltage is 10V. Find I_D?



(A) 0.35mA

(B) 0.25mA

(C) 0.40mA

(D) 0.45mA

Type: 3 Op-Amp

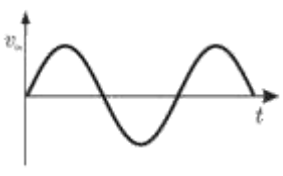
For Concept, refer to Analog Electronics K-Notes, Op-Amp

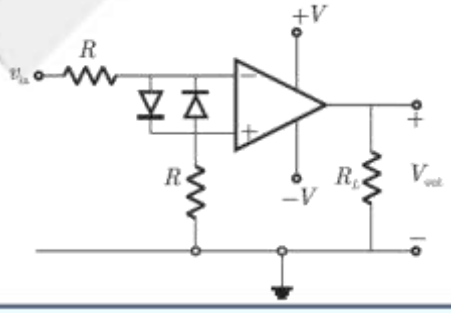
Point to Remember:

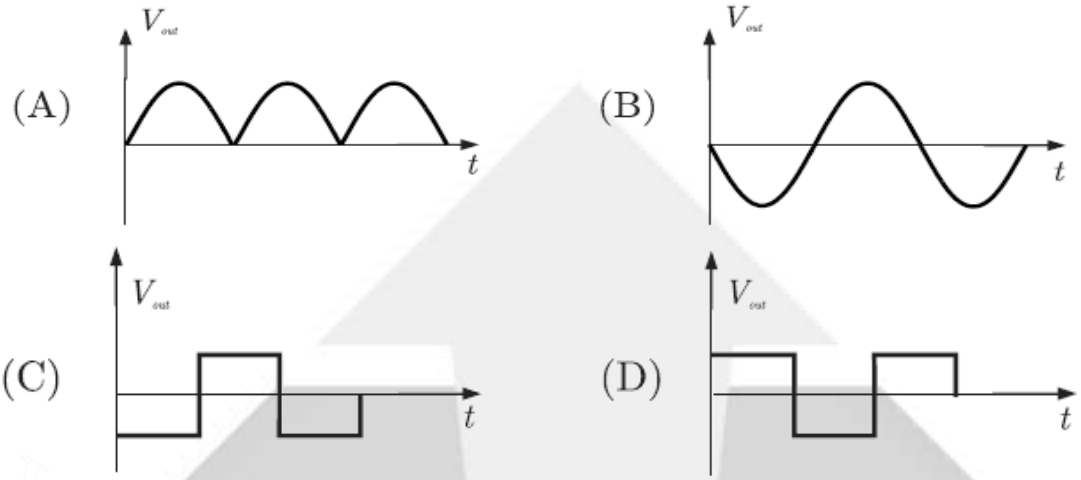
Before applying Virtual Ground Concept, check for Negative Feedback in the circuit.

Sample Problem 5:

In the given figure, if the input is a sinusoidal signal, the output will appear as shown







Solution: (C) is correct option
Since there is no feedback in the circuit and ideally op-amp has a very high value of open loop gain, so it goes into saturation (output is either +V or −V) for small values of input. The input is applied to negative terminal of op-amp, so in positive half cycle it saturates to −V and in negative half cycle it goes to +V .

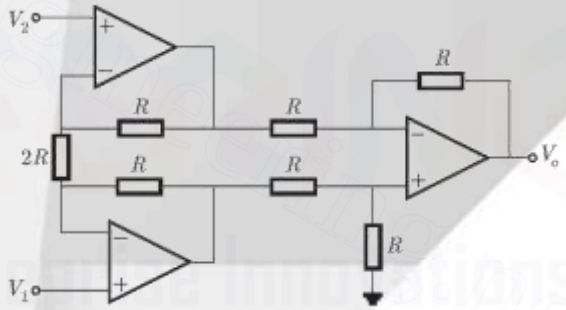
Sample Problem 6:
Given that the op-amps in the figure are ideal, the output voltage *V*0 is

(A) $(V_1 - V_2)$

(B) $2(V_1 - V_2)$

(C) $(V_1 - V_2)/2$

(D) $(V_1 + V_2)$



Solution: (B) is correct option
Voltage at "-" terminals of OP-Amp are also V_1 & V_2 by virtual ground concept.

$$I = \frac{(V_1 - V_2)}{2R}$$

$$V_- = V_2 - IR$$

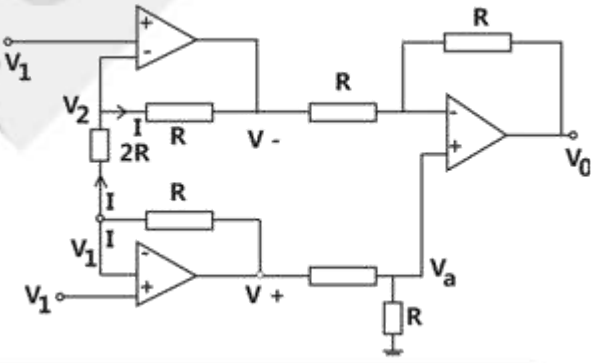
$$= V_2 - \frac{(V_1 - V_2)}{2R} \times R = \frac{(3V_2 - V_1)}{2}$$

$$V_+ = V_1 + IR$$

$$= V_+ = V_1 + \frac{(V_1 - V_2)}{2R} \times R = \frac{(3V_1 - V_2)}{2}$$

If only V_+ is present

$$V_a = \frac{V_+}{2} = \frac{(3V_1 - V_2)}{4}$$



$$V_0 = \left(1 + \frac{1}{1}\right)V_+ = \frac{(3V_1 - V_2)}{2}$$

If only V_- is present

$$V_0 = \frac{-1}{1} \times V_- = -\frac{(3V_2 - V_1)}{2}$$

$$\therefore V_0 = \frac{(3V_1 - V_2)}{2} - \frac{(3V_2 - V_1)}{2}$$

$$\left[V_0 = 2(V_1 - V_2)\right]$$

Unsolved Problems:

Q.1 If the differential voltage gain and common mode voltage gain of a differential amplifier are 100 dB and 10 respectively, then its common mode rejection ratio is

(A) 110 dB
(B) 90 dB
(C) 80 dB
(D) 10 dB

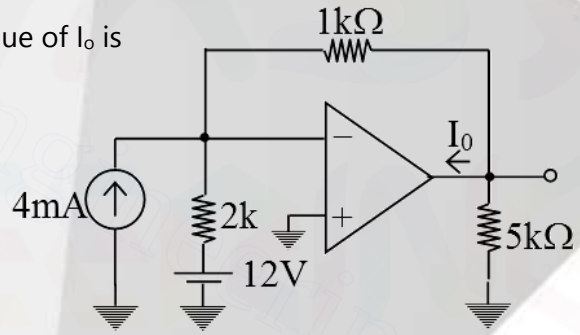
Q.2 For the op-amp circuit shown below, the value of I_o is

(A) 0 mA

(B) 2 mA

(C) 10 mA

(D) 12 mA



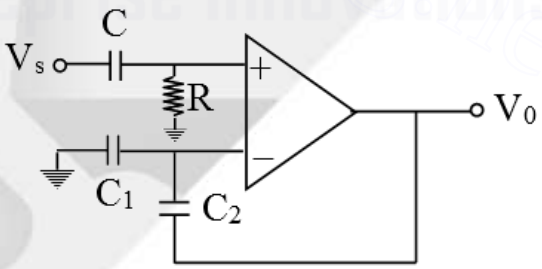
Q.3 The op-amp circuit shown below behaves as a

(A) High Pass filter

(B) Band Pass filter

(C) Integrator

(D) All Pass filter



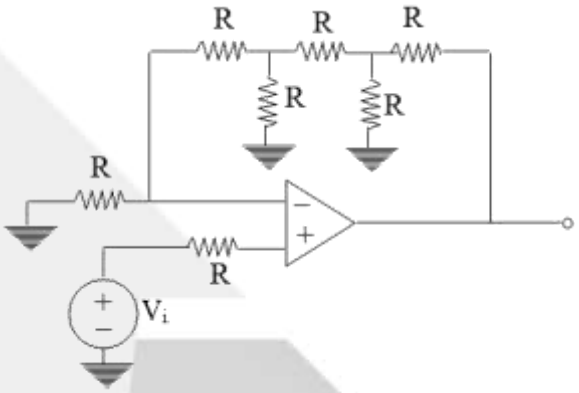
Q.4 . For the OP-amp shown below, the gain

(A) -8

(B) 13

(C) 5

(D) -10



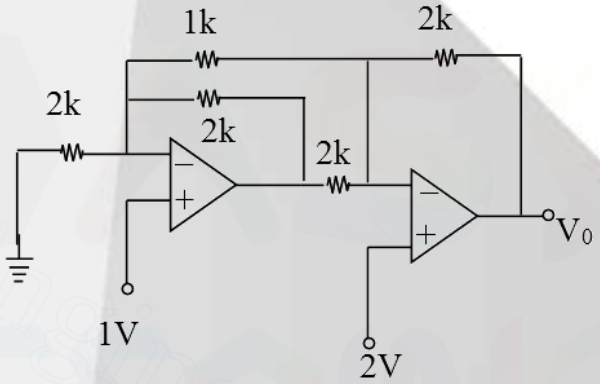
Q.5 The output (V_0) in the ckt shown in fig, assuming the op – amps as ideal

(A) 3 V

(B) 6 V

(C) 9 V

(D) 12 V



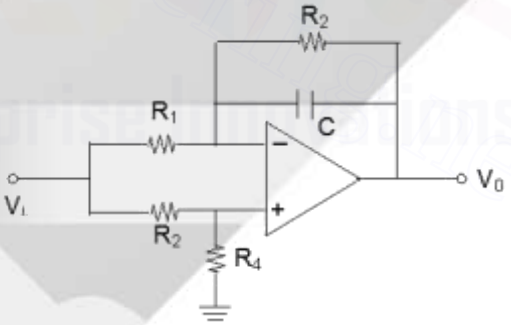
Q.6. In the op – Amp ckt shown in fig, If $R_1 = R_2 = R_A$ & $R_3 = R_4 = R_B$, the ckt acts as

(A) Sub tractor

(B) Integrator

(C) High pass filter

(D) Narrow band pass filter



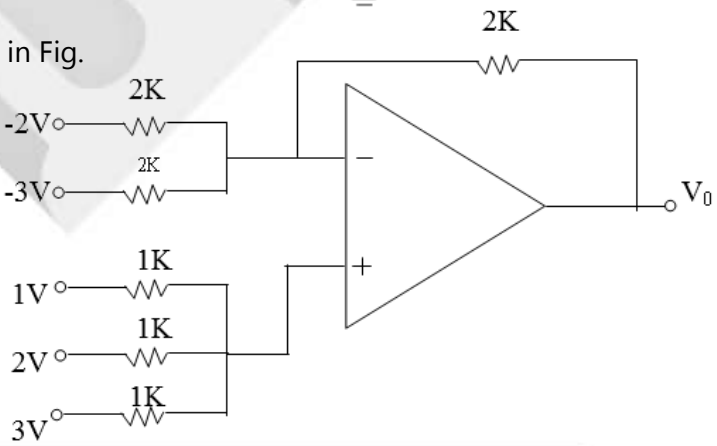
Q.7 The O/P voltage for the circuit shown in Fig.

(A) 1 V

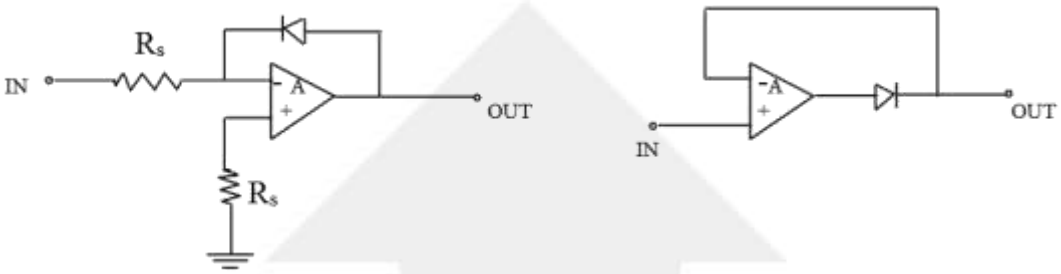
(B) 6 V

(C) 11 V

(D) 2 V



Q.8 The circuit connections of OP AMP given in figures (i) and (ii) represent



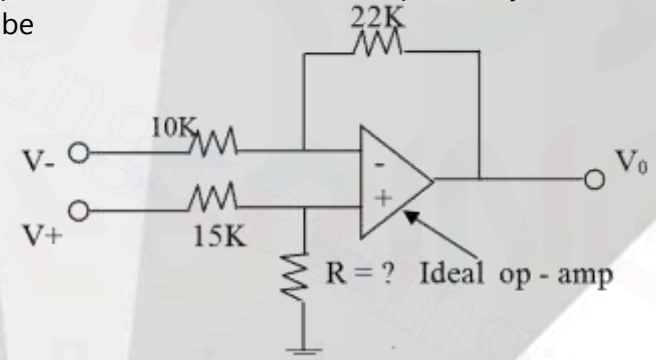
(A) logarithmic amplifiers for both figures (i) and (ii)

(B) detectors for both figures (i) and (ii)

(C) detector for figure (i) and logarithmic amplifier for figure (ii)

(D) logarithmic amplifier for figure (i) and detector for figure (ii)

Q.9 In the given circuit, if the voltage inputs V- and V+ are to be amplified by the same amplification factor, the value of R should be



(A) R=33k

(B) R=12k

(C) R=58k

(D) R=22k

Type: 4 Oscillators

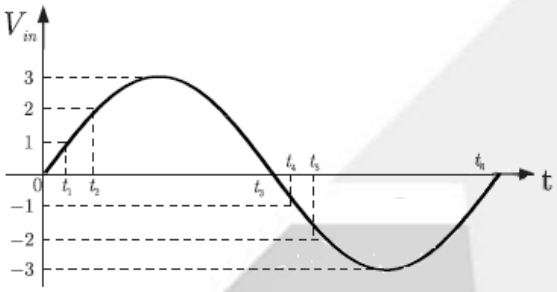
For Concept, refer to Analog Electronics K-Notes, Op-Amps

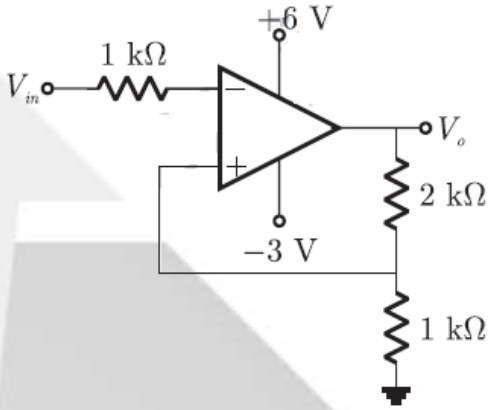
Point to Remember:

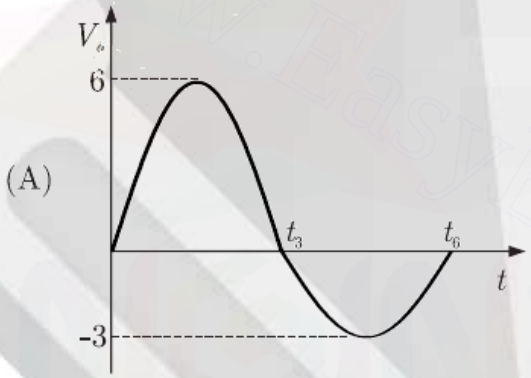
Instead of memorizing formulas for Schmitt Trigger better solve Oscillator circuit from scratch.

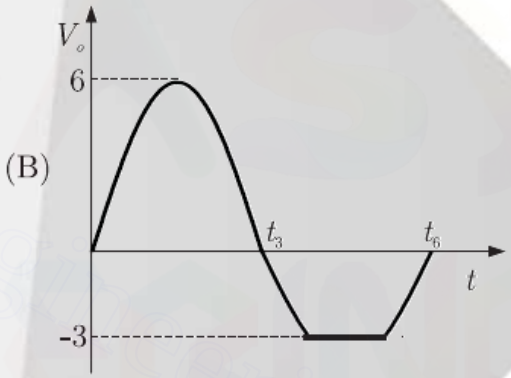
Sample Problem 7:

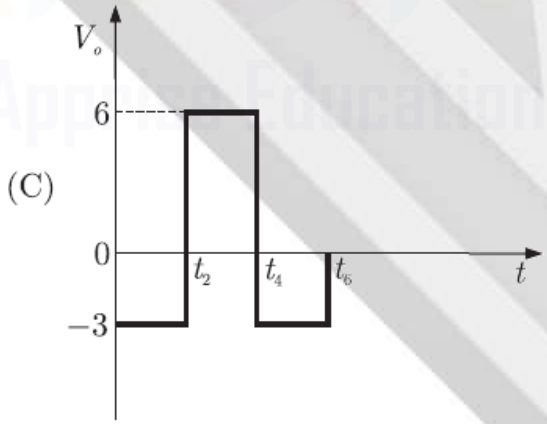
An ideal op-amp circuit and its input wave form as shown in the figures. The output waveform of this circuit will be

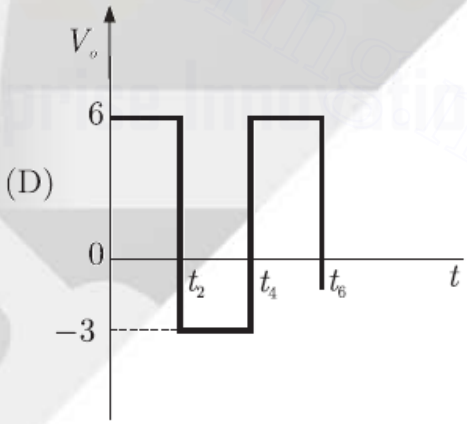












Solution: (D) Is correct option

Given that V_{sat}=6V, and $-V_{sat=-3V}$

Where V_0=+6V, the potential at non-inverting terminal is

$$V_{UTP} = +V_{sat}\left(\frac{R_2}{R_1+R_2}\right) = 6\left(\frac{1}{3}\right) = 2V$$

At instantaneous value of V_1=2V, V_0=+6V

If $V_{UTP} > V_i \Rightarrow V_0 = +6V$
$V_{UTP} < V_i \Rightarrow V_0 = -3V$

When V_0=-3V, the potential at non-inverting terminal is

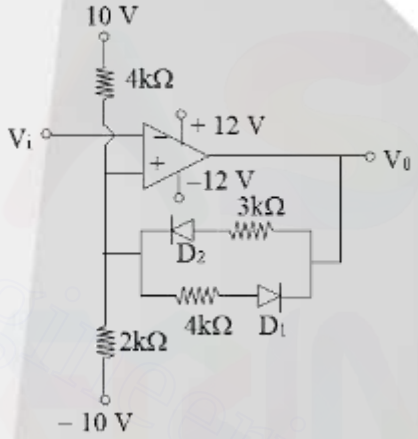
$$V_{LTP} = -3\left(\frac{1}{3}\right) = -1V$$

At $t<t_0$, $V_0 = -3V$ i.e. $V_{LTP} < V_i$

when $V_{LTP} > V_i \Rightarrow V_0 = +6V$

Unsolved Problems:

Q.1 For the Schmitt trigger circuit shown below, assume that op-amp and diodes are ideal. Then the values of the input voltage for positive going and negative going of hysteresis loop are



(A) – 5.5 V and 1.385V

(B) 5.5 V and –1.385 V

(C) –1.2 V and 10.67 V

(D) 1.2 V and –10.67 V

Q.2 In a Schmitt trigger the output v_0 is limited by Zener diodes. Signal v_S is connected to the negative input terminal (v_) and $v_+ = \beta v_0$. The Hysteresis voltage is 1 volt. Triggering takes place for signals going through

(A) zero volt
(B) 0 volt and + 1 volt
(C) 0 volt and – 1 volt
(D) + 0.5 volt and – 0.5 volt

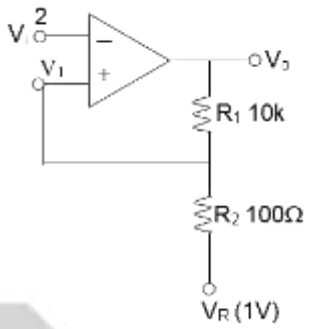
Q.3 In a Schmitt trigger using OP amplifiers the output is limited by Zener diode clipper to $v_0 = \pm 8$ volts. The positive input terminal voltage $v_+ = \beta v_0$, where $\beta = 1/8$. The signal v_s is applied v_. The following statements (1) to (4) are made regarding v_s and v_+.

1. For v_S negative and rising $v_+ = +1$
2. For v_S positive and decreasing $v_+ = +1$
3. For v_S decreasing through zero value $v_+ = +1$
4. For v_S increasing through zero $v_+ = +1$

Of these statements, the true statements are

(A) 1 and 3
(B) 2 and 3
(C) 1 and 4
(D) none of these statements

Q.4 The circuit of Schmitt trigger of fig., the hysteresis V_H is Assume if $V_i < V_1$, $V_0 = +5V$.



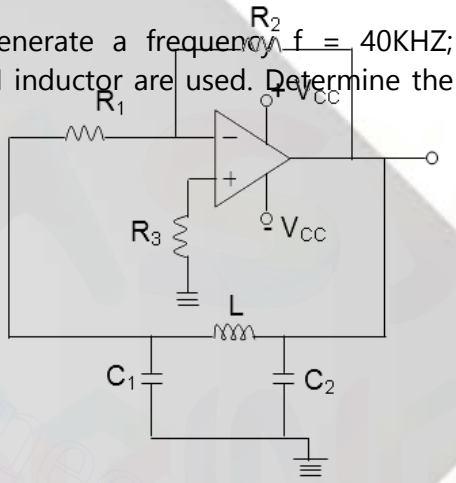
(A) 0.10V

(B) 0.25V

(C) 0.15V

(D) 0V

Q.5 Figure shows an oscillator circuit designed to generate a frequency f = 40KHZ; operation amplifier with a supply of = ±10V and 100mH inductor are used. Determine the value of C_2 for $C_1 = 10C_2$.



(A) 177PF

(B) 182PF

(C) 147PF

(D) 132PF

Type: 5 Digital Basics

For Concept, refer to Digital Electronics K-Notes, Number System and Boolean Algebra

Point to Remember:

Try to avoid redundant terms while calculating minimized logic using K-Map.

Sample Problem 8:

The SOP (sum of products) form of a Boolean function is $\sum(0,1.3.7.11)$, where inputs are A, B, C, D(A is MSB, and D is LSB). The equivalent minimized expression of the function is

(A) $(\bar{B}+C)(\bar{A}+C)(\bar{A}+\bar{B})(\bar{C}+D)$

(B) $(\bar{B}+C)(\bar{A}+C)(\bar{A}+\bar{C})(\bar{C}+D)$

(C) $(\bar{B}+C)(\bar{A}+C)(\bar{A}+\bar{C})(\bar{C}+\bar{D})$

(D) $(\bar{B}+C)(A+\bar{B})(\bar{A}+\bar{B})(\bar{C}+D)$

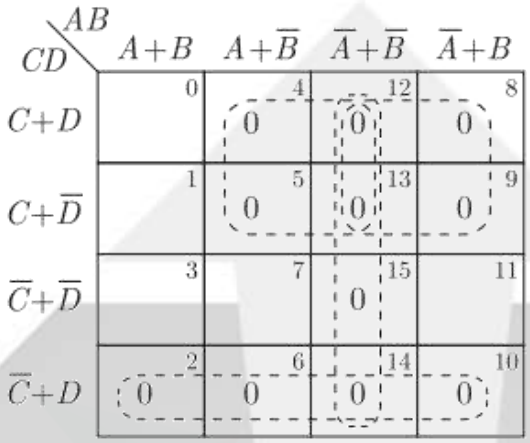
Solution: (A) is correct option

SOP Form, $F=\sum(0,1.3.7.11)$

POS Form, $F=\prod(2,4,5,6,8,9,10,12,13,14,15)$

Now we represent the POS form on the k-map

Here we enter 0's in those cells correspond to the max terms present in the given POS function.



So, $F_{min} = (\bar{B} + C)(\bar{A} + C)(\bar{A} + \bar{B})(\bar{C} + D)$

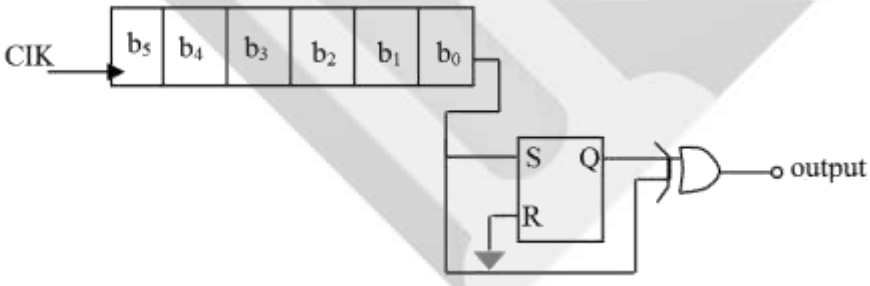
Unsolved Problems:

Q.1 What is the decimal value of 2's comp no 111110100001

(A) + 123
(B) -95
(C) -107
(D) -122

Q.2 How many two input NOR gates are required to implement the Boolean Functions
F = $\overline{(A+B)(C+D)}$
(A) 5
(B) 4
(C) 3
(D) 6

Q.3 A 5 – bit binary number is stored in the shift register and connected to D – FF as shown below. Determine the function of the circuit is



(A) Binary to Gray code converter
(B) Gray to Binary code converter
(C) 1's complement of Binary no.
(D) 2's complement of Binary number

Q.4 Pick the correct statements.

P: Base r system will have r's and (r-1)'s complements
Q: In 1's complement representation, we can represent more numbers
R: 2's Complement representation has A symmetric representation
S: Range of numbers represented in sign magnitude form is $+(2^{n-1}-1)$ to -2^{n-1}.
T: 1's complement representation of –7 to 1000.
U: Digital computers implement 2's complement representation

(A) P, R, T, U
(B) Q, R, T
(C) P, Q, R, T, U
(D) Q, R, S, T

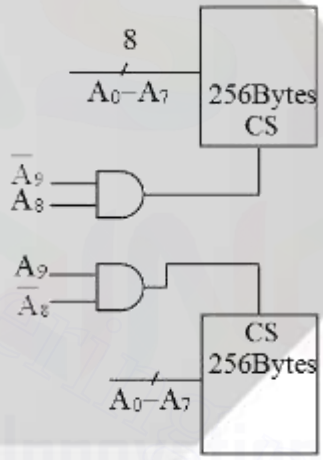
Q.5 Which of the following is not the address of the memory shown in figure.

(A) $0100_H - 02FF_H$

(B) $FE00_H - FFFF_H$

(C) $8900_H - 8AFF_H$

(D) $CD00_H - CEFF_H$



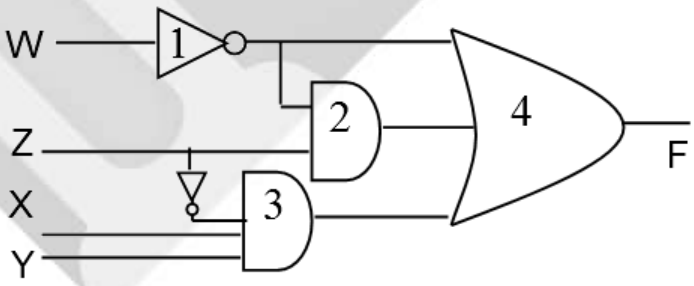
Q.6 In the following logic circuit, which gate is reductant

(A) 1

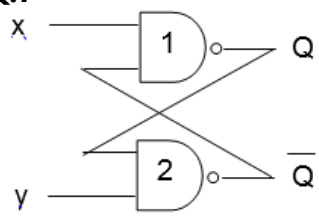
(B) 2

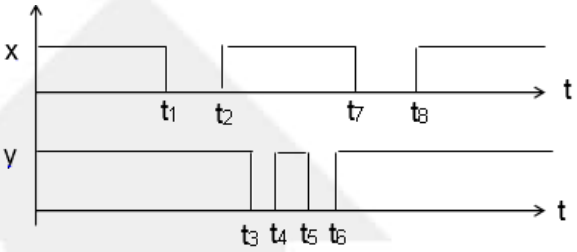
(C) 3

(D) 4



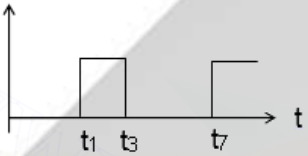
Q.7





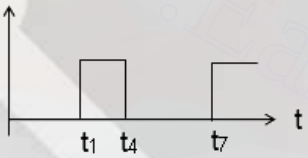
Output wave form at Q is

(A)

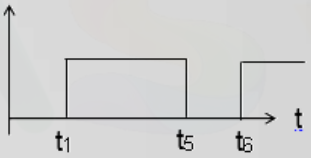


(B)

(C)



(D)



Q.8 A Full Adder is constructed using number of EX-OR gates, AND gates and OR gates. The propagation delays of the gates are as shown below.

EX-OR	:	20 ns
AND	:	10 ns
OR	:	10 ns

Assume data inputs A_n, B_n and carry C_{n-1} are applied simultaneously.
The number EX-OR, OR and AND gates required are

(A) 2,2,1
(B) 2,2,2
(C) 1,2,1
(D) 2,1,2

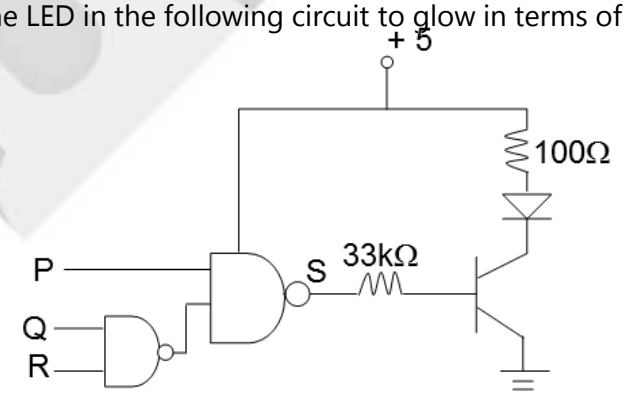
Q.9 Derive the logical expression for 'S' for the LED in the following circuit to glow in terms of P, Q and R.

(A) PQ + QR + PR

(B) PQR

(C) $\overline{P}$ + QR

(D) P + Q + R



Type: 6 Sequential and Combinational Circuits

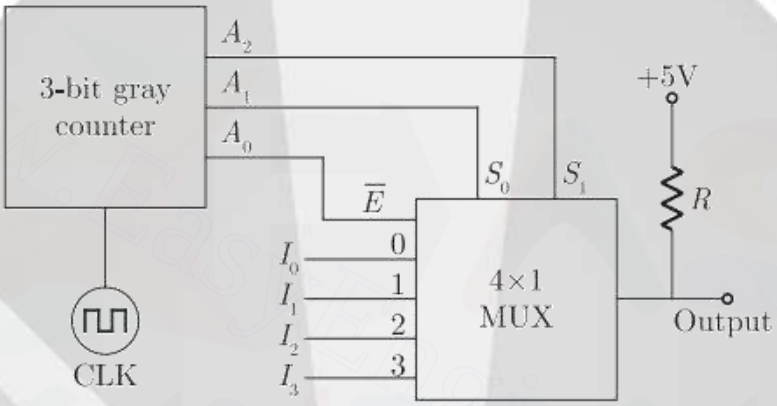
For Concept, refer to Digital Electronics K-Notes, Combinational Logic Circuits and Sequential Logic Circuits.

Point to Remember:

Remember characteristic equation of all Flip Flops to solve problems.

Sample Problem 9:

A 3-bit gray counter is used to control the output of the multiplexer as shown in the figure. The initial state of the counter is 000_2. The output is pulled high. The output of the circuit follows the sequence



(A) I_0, 1, 1, I_1, I_3, 1, 1, I_2
(B) I_0, 1, I_1, 1, I_2, 1, I_3, 1
(C) 1, I_0, 1, I_1, I_2, 1, I_3, 1
(D) I_0, I_1, I_2, I_3, I_0, I_1, I_2, I_3

Solution: (A) is correct option
Initial state of gray counter is $(000)_2$. So, we have the outputs
$A_0 = 0$ and $A_1=0$ and $A_2=0$
For the enable input to multiplexer, we have
If $\overline{E} = 0$, then it will select any one of I_0, I_1, I_2, I_3.
If $\overline{E} = 1$, then it will be in high impedance state.
So, we get the output of multiplexer for the different inputs (output of 3-bit gray counter) as

Initial counter	output
000	I_0
001	1 (High impedance state)
011	1 (High impedance state)
010	I_1
110	I_3
111	1 (High impedance state)
101	1 (High impedance state)
100	I_2

Unsolved Problems:

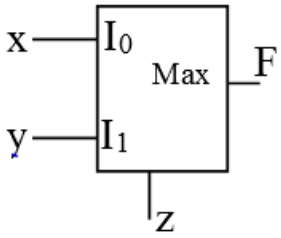
Q.1 A 2:1 multiplexer is used to represent the Boolean Function $F(A,BC) = AB + \overline{A}C + BC$ Determine the values of x, y and z

(A) x = A ; y = B, z = C

(B) x = B ; y = C ; z = A

(C) x = C ; y = B ; z = A

(D) x = B ; y = 1 ; z = A



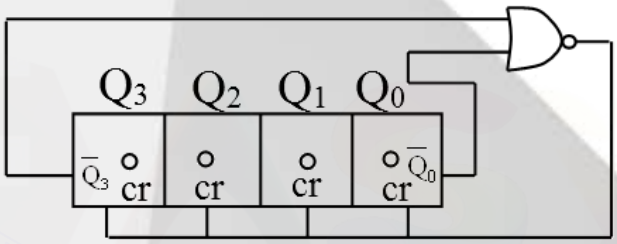
Q.2 What is the modulus of the following counter

(A) 8

(B) 10

(C) 7

(D) 9



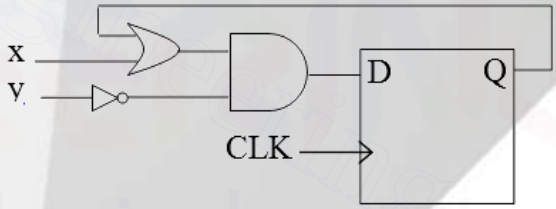
Q.3 Determine the characteristic equation of the X – Y FF shown below.

(A) $\overline{x}.\overline{Q}+y.Q$

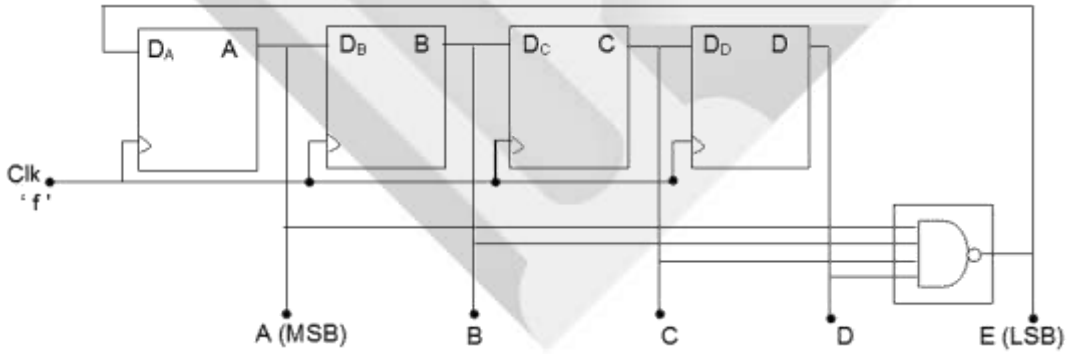
(B) $x.\overline{y}+Q.\overline{y}$

(C) $x.y+\overline{y}.Q$

(D) $\overline{x}.\overline{Q}+y.Q$



Q.4 Consider the following digital circuit



What is the counting sequence in decimal of the above circuit.

(A) 25, 29, 17, 1, 3, 4

(B) 29, 17, 30, 6, 14, 5

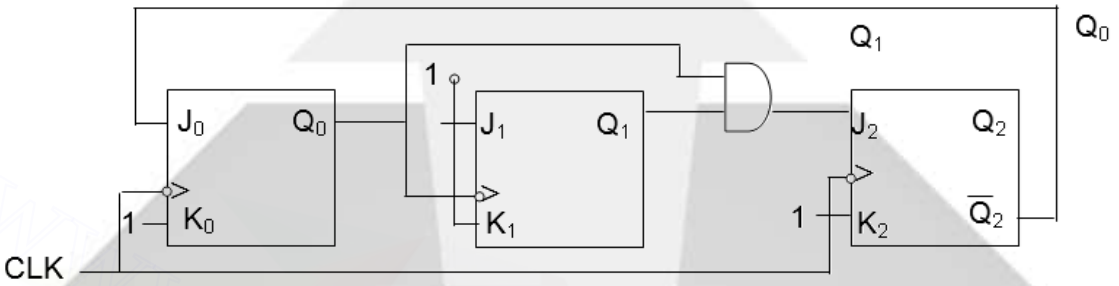
(C) 25, 17, 19, 25, 24, 13

(D) 29, 30, 14, 23, 27

Q.5 In a 8–bit parallel Binary Adder, the time taken to produce the sum and carry outputs of full adder are 32ns and 24ns respectively. What are the maximum number additions per second that it can perform?

(A) 1×10^6 (B) 8×10^4
(C) 5×10^6 (D) 4×10^8

Q.6 A mod – 5 counter shown below counts through states $Q_2\ Q_1\ Q_0$ = 000, 001, 010 and 100



Find the maximum rate at which the counter will operate satisfactorily. The Propagation delay of each flip flop is 10 ns. Neglect prop delay of AND gate

(A) 100 MHz (B) 50 MHz
(C) 10 MHz (D) 5 MHz

Q.7 In a 4 bit modulo-6 ripple counter the proportional delay of J-K Flip flop is 50 ns. What is the max. clock frequency that can used without skipping a count.

(A) 2 MHz (B) 4 MHz
(C) 5 KHz (D) 5 MHz

Q.8 A sequential circuit designed using J – K flip flops is described by the following state equation. What are the inputs J_A, K_A.

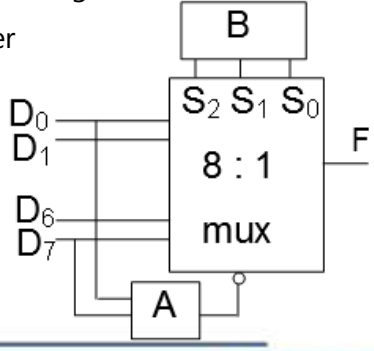
$$A(t + 1) = x\,AB + y\,A'\,C + xy$$

(A) $J_A = x'\,B + yCB'$, $J_B = A'\,B' + xB$ (B) $J_A = yx'\,C + yB'$ $J_B = xy'\,C + x'\,B'$
(C) $J_A = yC + xy$ $K_A = x' + y'\,B'$ (D) $J_A = 1$ $K_A = y'\,B'$

Q.9 In the following 8 : 1 multiplexer if D_0 and D_7 inputs are identical no data inputs are to be connected to the output and so long D_0 and D_7 are different D_7 through D_0 are connected continuously in succession to the output. Identify the gates at 'A' and digital circuit at 'B'.

(A) NOR, 3 – bit up counter (B) EX – NOR, 3 bit up counter

(C) EX – OR, 3 – bit down counter (D) NAND, 3 – bit counter



Type: 7 A/D & D/A Converters

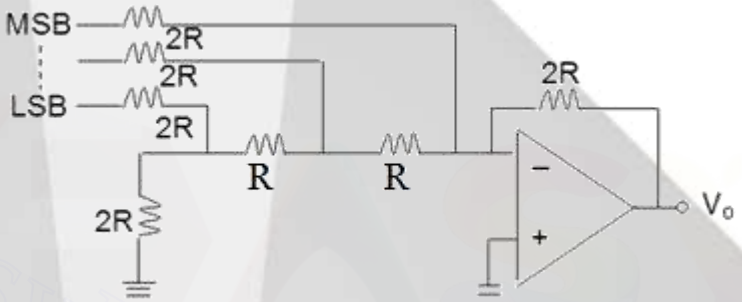
For Concept, refer to Digital Electronics K-Notes, A/D and D/A Converters.

Point to Remember:

Memorize the maximum time of conversion of various ADCs.

Sample Problem 10:

What is the Resolution of the following Digital – to – Analog converter if '1' = 5V and '0' = 0.V.



(A) 2.5V

(B) 0.625V

(C) 1.25V

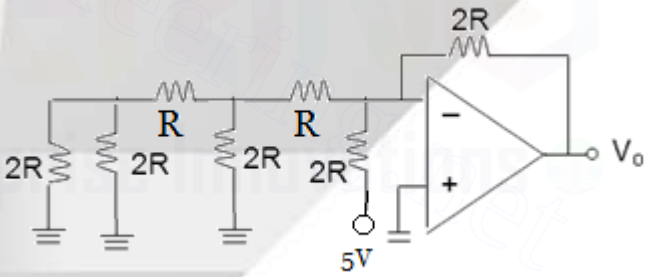
(D) 3.75V

Solution: (C) is correct option

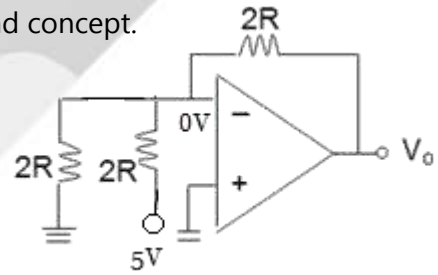
This is a 3-bit converter. Assume input as (100) that is the MSB is equated to 1 and other bits are zero.

The decimal equivalent of this binary number is "4"

The circuit then looks like:



If we simplify the circuit then it becomes:



The voltage at inverting terminal is 0V due to virtual ground concept.

Therefore grounded resistance can be neglected.

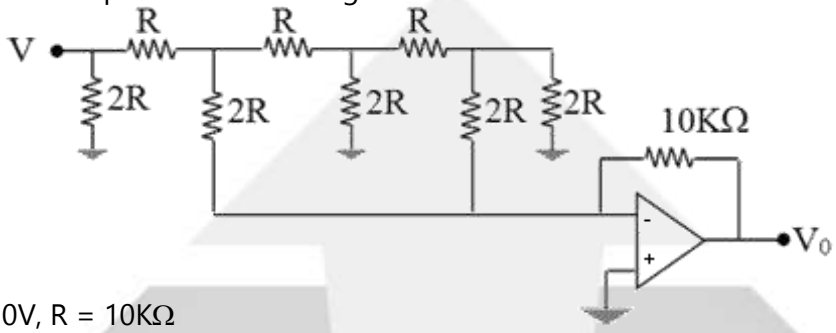
The circuit works as Inverting Amplifier with output = -5V

Resolution = Analog Output/ Decimal Input

= 5/4 = 1.25V

Unsolved Problems:

Q.1 What is the output of the following current switched DAC.



Given V = 10V, R = 10KΩ

(A) –6.5V
(B) + 7.25 V
(C) –6.25V
(D) – 3.125V

Q.2 A 8-bit counter type ADC has a clock frequency of 10 MHz and the DAC is controlled by the equation $\sum_{i=0}^{7} 2^{n-2}.b_n$ Its input voltage range is $-10V \text{ to } +10V$. Determine the output for an analog input of 3.2 volts

(A) 00001001
(B) 00001101
(C) 11001010
(D) 00001111

Q.3 A D/A connecter has 10 v full scale output voltage and an accuracy of ± 0.2%. The maximum error for any output voltage will be

(A) 5 mv
(B) 20 mv
(C) 10 mv
(D) 25 mv

Q.4 Which of the following statements are correct
(i) In dual slope ADC, the speed of conversion is more.
(ii) In Flash type ADC, as the size increases the hardware complexity increases
(iii) In successive approximation ADC, the conversion time depends on magnitude of input.
(iv) Continuous time signals can't be converted to digital by using only ADC.

(A) i, ii, iii
(B) ii, iv
(C) iii, iv
(D) i, iv

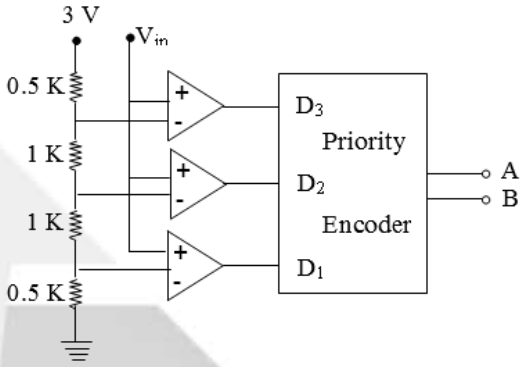
Q.5 In the 2-bit ADC shown below, if the analog input V_{in} is in the range $1.5 < V_{in} < 2.5$ V, then the Digital output is

(A) 11

(B) 10

(C) 01

(D) 00



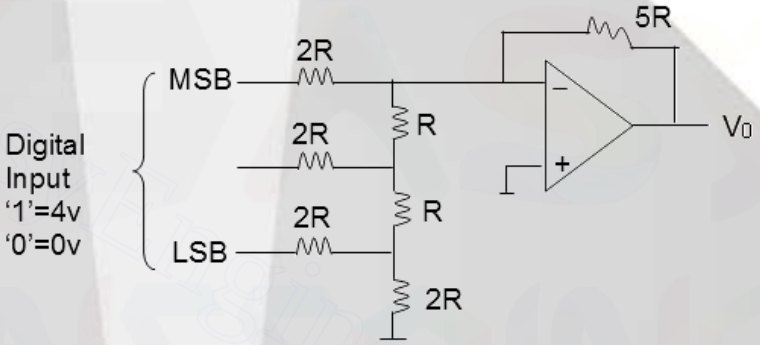
Q.6 What is the output of the following DAC when the digital Input is 010.

(A) 4 V

(B) 5 V

(C) – 5 V

(D) – 4V



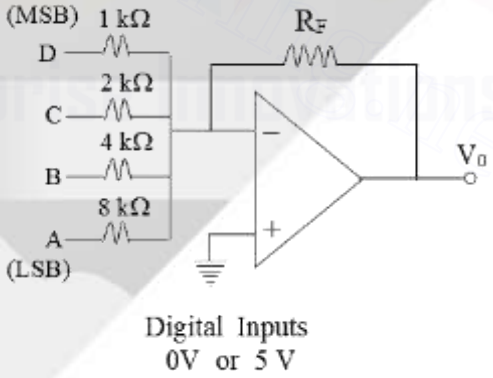
Q.7 The step size of the DAC shown in figure is 0.5V. The value of R_F is

(A) 1 kΩ

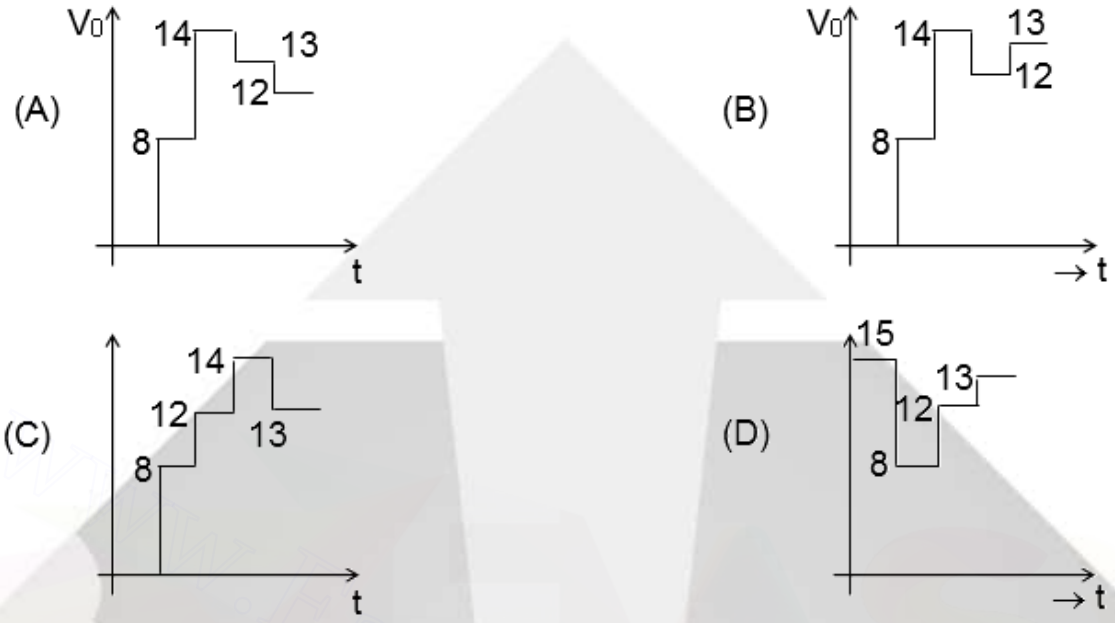
(B) 8 kΩ

(C) 10 kΩ

(D) 800 Ω



Q.8 Consider a 4 – bit successive approximation Register output is fed to DAC. Whose step size is 1V. The Full Scale output of DAC is +15V. Which of the following waveforms indicate the output of DAC. When the analog input is 13V.



Type: 8 Microprocessor

For Concept, refer to Digital Electronics K-Notes, Microprocessor

Point to Remember:

Memorize the bits affected by each instruction as that will be used in Conditional Jump Instructions.

Sample Problem 11:

In an 8085 microprocessor, the following program is executed

Address location Instruction

2000H XRA A

2001H MVI B, 04H

2003H MVI A, 03H

2005H RAR

2006H DCR B

2007H JNZ 2005

200AH HLT

At the end of program, register A contains

(A) 60H (B) 30H

(C) 06H (D) 03H

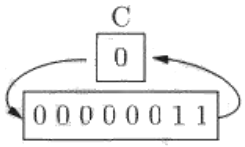
Solution: (A) is correct option

XRA A ⟶ A ⟵ 00H Ex-OR (operation with accumulate)

2001H MVI B, 04H B ⟵ 04H (04H started in B)

2003H MVI A, 03H A ⟵ 03H (03H started in A)

2005H RAR rotate accumulator right with carry



2006H DCR B B ← 03H (B decremented by one)
2007H JNZ 2005 Jump to 2005H till B not comes equal to zero
So

B	C	A
03H	1	01H
02H	1	80H
01H	0	COH
00H	0	60H

Unsolved Problems:

Q.1 How many times NOP is executed

```
        MVI A, 10 H
        MVI B, 10 H
Back :  NOP
        ADD B
        RLC
        JNC Back
        HLT
```

(A) 2 (B) 1
(C) 3 (D) 4

Q.2

```
1   XRA  A
2   LXI  H, 12 F3H
3   LXI  D, FF 27 H
4   XCHG
5   INX  H
6   MOV  A, L
7   ADD  H
8   ORA  A
9   Push  PSW
10  Pop B
11  HLT
```

What are the values of ACC and Flag register?
(A) 28 H, 14 H (B) 27 H, 14 H
(C) 28 H, 04 H (D) 27 H, 24 H

Q.3 Pick the correct statements

P. In I/o, microprocessor can have 256 input, 256 output devices

Q. In memory mapped I/o, the address of a peripheral is 8 bits

R. In memory mapped I/o, the control signals used for peripherals are IOW, IOR

S. In I/o mapped I/o, the hardware complexity is less for peripheral interface

T. Control signal Io/ m is not required in memory mapped I/o operation

(A) Q, S, T
(B) P, R, T
(C) Q, R, T
(D) P, S, T

Q.4 After the execution of the following routine, what are the contents of memory locations 9000 H, 9001H.

```
LXI SP, 2400H
MVI L, 01H
XRA  A
CMA
MOV H,A
DAD SP
SHLD 9000
HLT
```

(A) 01, 23
(B) FF, 23
(C) 01, 24
(D) FF, 24

Q.5 Write ALP to store 5 D_H in the flag register of 8085 microprocessor. The data in the other registers should not change in the above process.

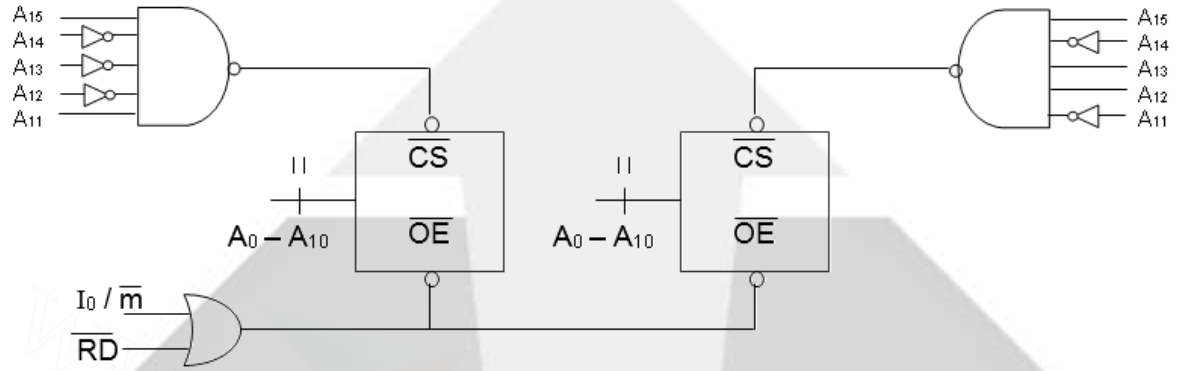
(A)
```
MVI A, 5D
MOV H, L
Push H
Pop PSW
```

(B)
```
MVI L, 5D
MOV H, A
Push H
Pop PSW
```

(C)
```
MVI L, A
MVI H, 5D
Pop PSW
```

(D)
```
MVI L, 5D
MOV A,
Push H
Pop PSW
```

Q.6 The memory is interfaced to microprocessor as shown below. What is address range of both memory chips.



(A) 8000 – 8FFF
B000 – B7FF
(B) 8800 – 8FFF
B800 – BFFF
(C) 8000 – 8FFF
B800 – BFFF
(D) 8800 – 8FFF
B000 – B7FF

Q.7 In a 8085 microprocessor the following instruction are executed and the its clock frequency is 2 MHz. Arrange the instructional according to their execution times in descending order.

(1) Push H (2) PCHL (3) XCHG (4) XTHL

(A) 4, 1, 2, 3
(B) 3, 2, 4, 1
(C) 4, 3, 1, 2
(D) 3, 4, 1, 2

Q.8 In 8085 microprocessor system, the data in some memory locations are as shown below. Determine the 'ACC' register contents at the end of the following program. Also determine the contents of HL register pair.

Address	Data	⇒	
8250	52		LHLD 8250 H
8251	82		MOV E,M
8252	50		INX H
8253	82		MOV D, M
			XCHG
			LDAX D

(A) 50, 8251
(B) 82, 8252
(C) 50, 8252
(D) 82, 8250

Q.9 Determine the contents of SP and HL registers after executing the following instructions stored starting from 3850H address location.

L x I SP, FFFF
CALL, 3856
POP H

(A) SP = FFFF, HL = 3850
(B) SP = FFFD, HL = 3850
(C) SP = FFFF, HL = 3856
(D) SP = FFFD, HL = 3856

Answer Key

	1	2	3	4	5	6	7	8	9
Type 1	B	B	B	C	B	C	B	B	B
Type 2	C	D	A	C	A	B	D	C	B
Type 3	C	D	A	B	B	C	C	D	A
Type 4	A	D	C	A	A				
Type 5	B	B	D	A	B	B	D	D	C
Type 6	B	D	B	D	C	B	D	C	C
Type 7	D	D	B	D	B	C	D	C	
Type 8	A	B	D	A	B	D	A	D	C

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